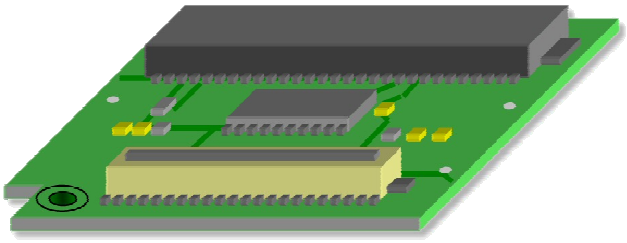


LX-18T-20H-31P ***LVDS Transmitter Datasheet*** **Version 1.00**

Description:

The LX-18T-20H-31P is designed to take standard Flat Panel Display TTL Level logic signals and convert them to LVDS for transmission to a Flat Panel Display equipped with either a Road Rage Labs LVDS Receiver or its own on-board LVDS receiver. Benefits include longer cable transmission length with reduced EMI emissions. These modules are designed for minimum size and maximum signal integrity. ROHS versions are available upon request.

These boards are designed to fit onto an existing single board computer that was designed to drive a TTL display. The LX-18T-20H-31P is outfitted with a standard connector (Hirose DF9-31 series) that will mate with many existing boards. TTL is adapted to LVDS for the added benefits that LVDS brings. On the receiving end – Road Rage offers several standard boards that can take the incoming LVDS signal and turn it back into TTL if you are driving an older TTL input LCD. Alternately, the LX-18T-20H-31P can drive any flat panel that uses a standard Single-Channel LVDS interface.

Custom cables for any application are available from Road Rage. Email or call for configuration options.

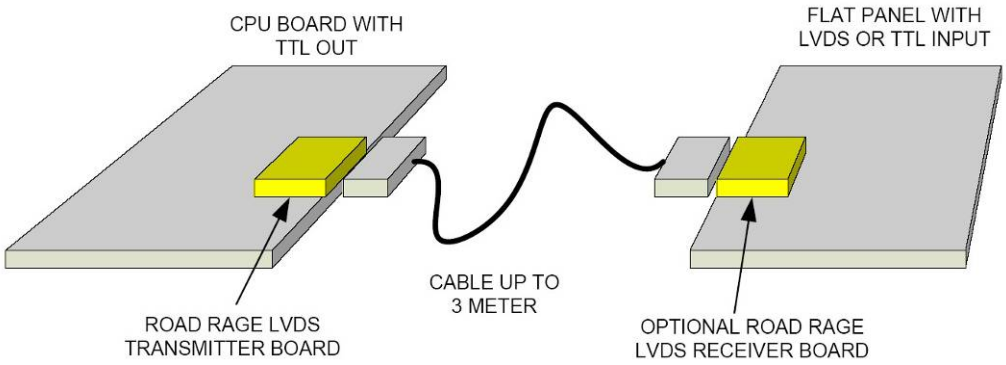


Figure 1: Typical System

LX-18T-20H-HR	Hirose
LX-18T-20HR-31P	Hirose (ROHS)
LX-18T-20M-31P	Molex
LX-18T-20MR-31P	Molex (ROHS)

Table 1: Part Versions

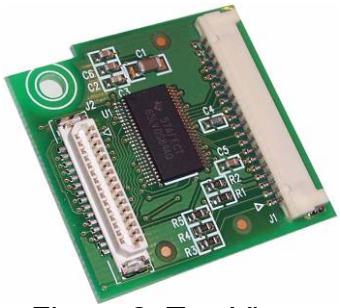


Figure 2: Top View

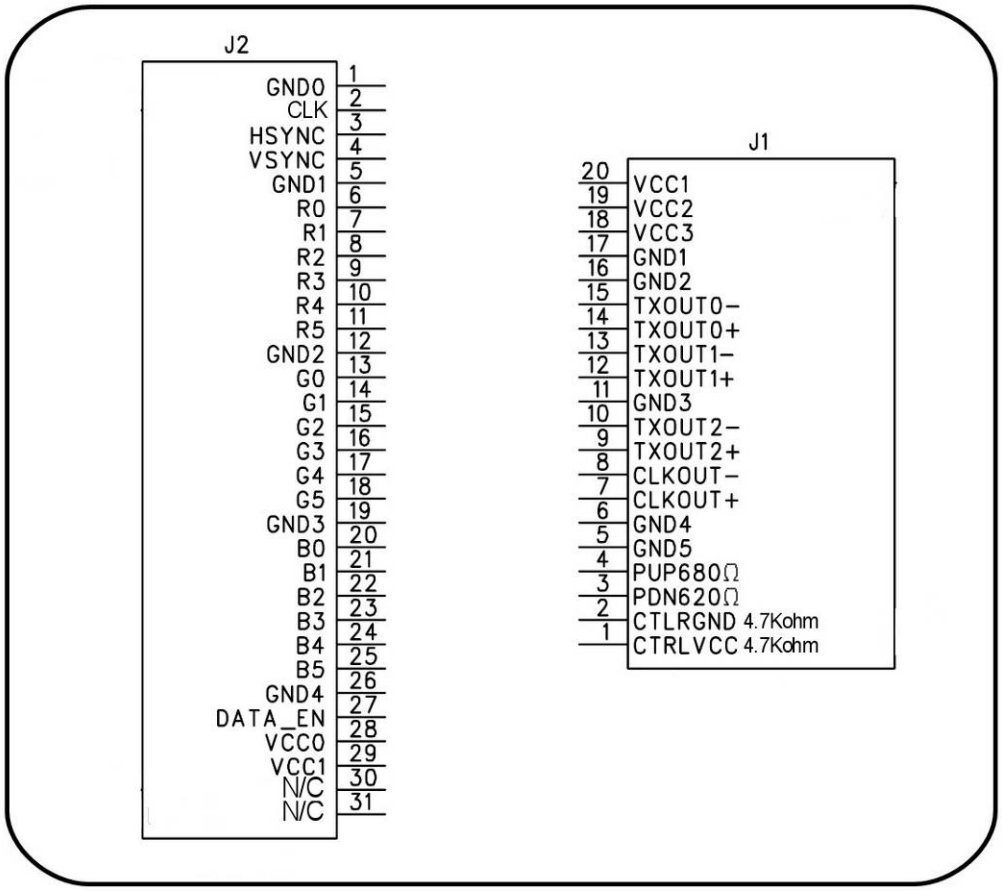


Figure 3: Input and Output Connector Pin out

Input Connector (J2)			
	Description	31pin 1mm SMT	
	Manufacturer	Hirose	
	Part Number	DF9*-31S-1V (32)	
	Mate Part Number	DF9*-31P-1V (32)	
	Height	4.3mm stack	
Output Connector (J1)			**Optional**
	Manufacturer	Hirose	Molex
	Description	20 pin 1.25mm SMT	20 pin 1.25mm SMT
	Part Number	DF14*-20P-1.25H (59)	53780-2070
	Mate Part Number	DF14-20S-1.25C DF14-2628 SCF A (pins)	51146-2000 50641/50753 (pins)
	Height	2.5mm	1.85mm

Table 2: Connector Specification Input and Output

LX-18T-20-**

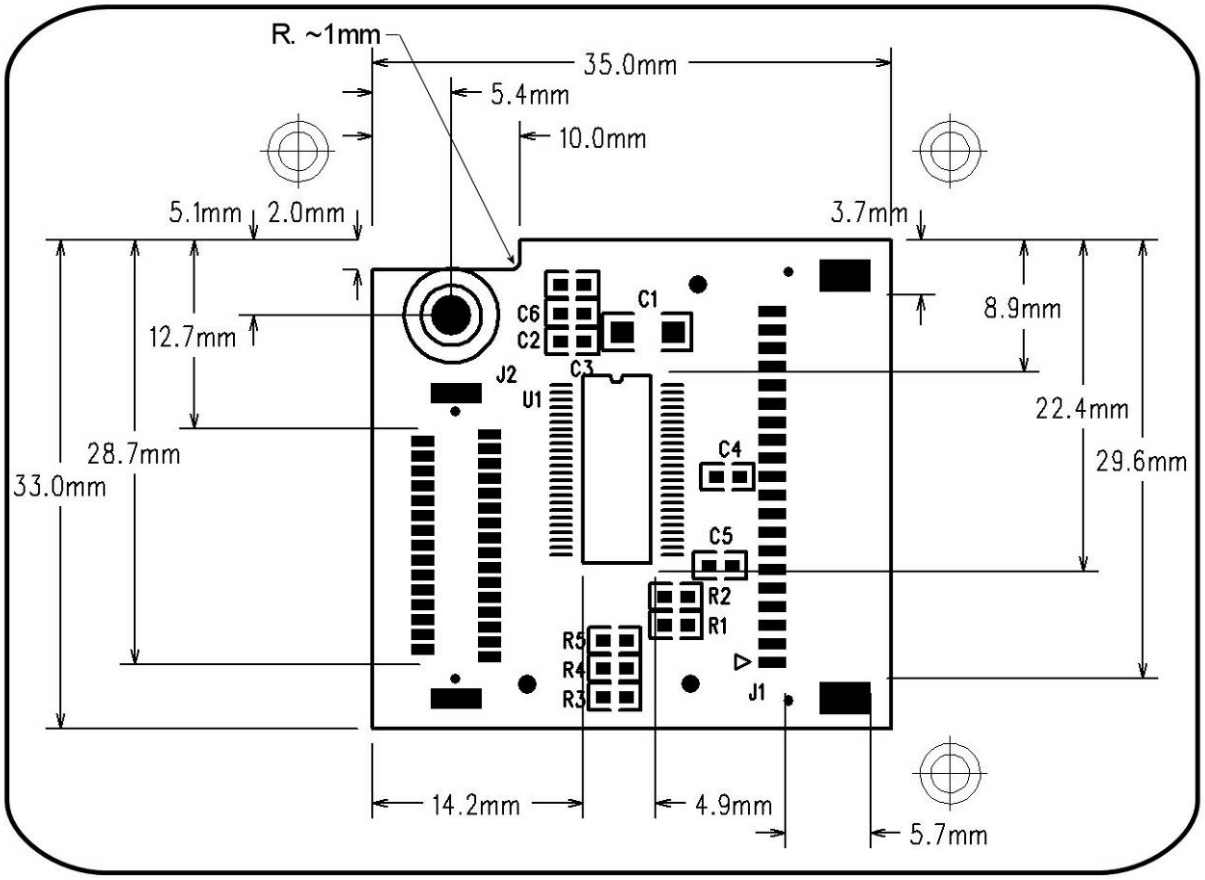
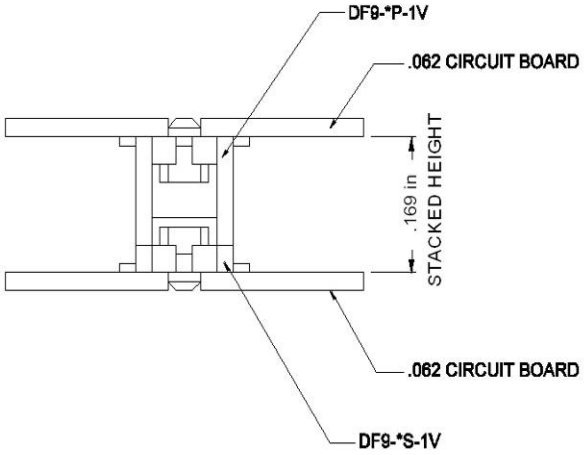


Figure 4: Board Mechanical - Top View



NOTE: THE BOARD TO BOARD SIZE .169 in (4.3mm) DOES NOT INCLUDE SOLDER THICKNESS

Figure 5: Board Mechanical - Stackup

LX-18T-20-**

Electrical Specifications	Min	Nom	Max	Unit
Operating Temp Range	-40		85	Deg C
Supply Voltage	3.0	3.3	3.6	Volts
Input High Level	2.0			Volts
Low-Level Input Voltage			.08	Volts

Table 3: Electrical Specifications

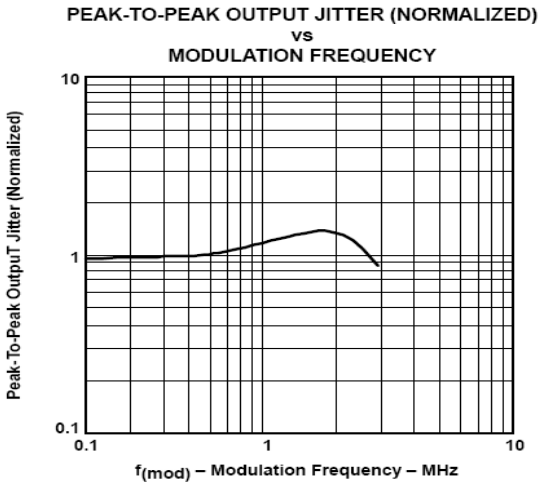


Figure 6: Out Jitter

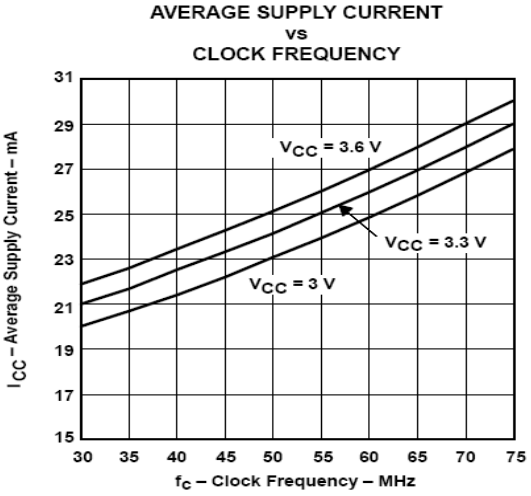


Figure 7: Supply Current

timing requirements

		MIN	NOM	MAX	UNIT
t_c	Input clock period	13.3	t_c	32.4	ns
t_w	Pulse duration, high-level input clock	$0.4t_c$		$0.6t_c$	ns
t_t	Transition time, input signal			5	ns
t_{su}	Setup time, data, D0 – D20 valid before CLKIN↓ (see Figure 2)	3			ns
t_h	Hold time, data, D0 – D20 valid after CLKIN↓ (see Figure 2)	1.5			ns

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT}	Input threshold voltage				1.4		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω, See Figure 3		247		454	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states					50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 100 Ω, See Figure 3		1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$	SN75LVDS84A			20	µA
			SN65LVDS84AQ			25	
I_{IL}	Low-level input current	V_{IL} = 0				±10	µA
I_{OS}	Short-circuit output current	$V_{O(Yn)}$ = 0			–6	±24	mA
		V_{OD} = 0			–6	±12	mA
I_{OZ}	High-impedance output current	V_O = 0 to V_{CC}				±10	µA
$I_{CC(AVG)}$	Quiescent supply current (average)	Disabled, All inputs at GND	SN75LVDS84A		15	150	µA
			SN65LVDS84AQ		15	170	
		Enabled, R_L = 100 Ω (4 places) Gray-scale pattern (see Figure 4)	f = 65 MHz		27	35	mA
			f = 75 MHz		30	38	
		Enabled, R_L = 100 Ω, (4 places) Worst-case pattern (see Figure 5)	f = 65 MHz		28	36	
			f = 75 MHz		31	39	
C_I	Input capacitance				2		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Table 4: Timing and Electrical Spec's

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{d0}	Delay time, CLKOUT↑ to serial bit position 0	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps‡, See Figure 6	−0.2		0.2	ns
t_{d1}	Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_c - 0.2$		$\frac{1}{7}t_c + 0.2$	
t_{d2}	Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_c - 0.2$		$\frac{2}{7}t_c + 0.2$	
t_{d3}	Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_c - 0.2$		$\frac{3}{7}t_c + 0.2$	
t_{d4}	Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_c - 0.2$		$\frac{4}{7}t_c + 0.2$	
t_{d5}	Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_c - 0.2$		$\frac{5}{7}t_c + 0.2$	
t_{d6}	Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_c - 0.2$		$\frac{6}{7}t_c + 0.2$	
$t_{sk(o)}$	Output skew, $t_n - \frac{n}{7}t_c$		−0.2		0.2	ns
t_{d7}	Delay time, CLKIN↓ to CLKOUT↑	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps‡, See Figure 6		2.7		ns
		t_c = 13.33 ns ~ 32.25 ns (± 0.2%), |Input clock jitter| < 50 ps‡, See Figure 6	1		4.5	
$\Delta t_{c(o)}$	Cycle time, output clock jitter§	t_c = 15.38 + 0.308 sin (2π500E3t) ± 0.05 ns, See Figure 7		±62		ps
		t_c = 15.38 + 0.308 sin (2π3E6t) ± 0.05 ns, See Figure 7		±121		
t_w	Pulse duration, high-level output clock			$\frac{4}{7}t_c$		ns
t_t	Transition time, differential output voltage (t_r or t_f)			700	1500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)			1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state (CLKOUT low)			6.5		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ |Input clock jitter| is the magnitude of the change in the input clock period.
§ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

Table 5: Switching Characteristics

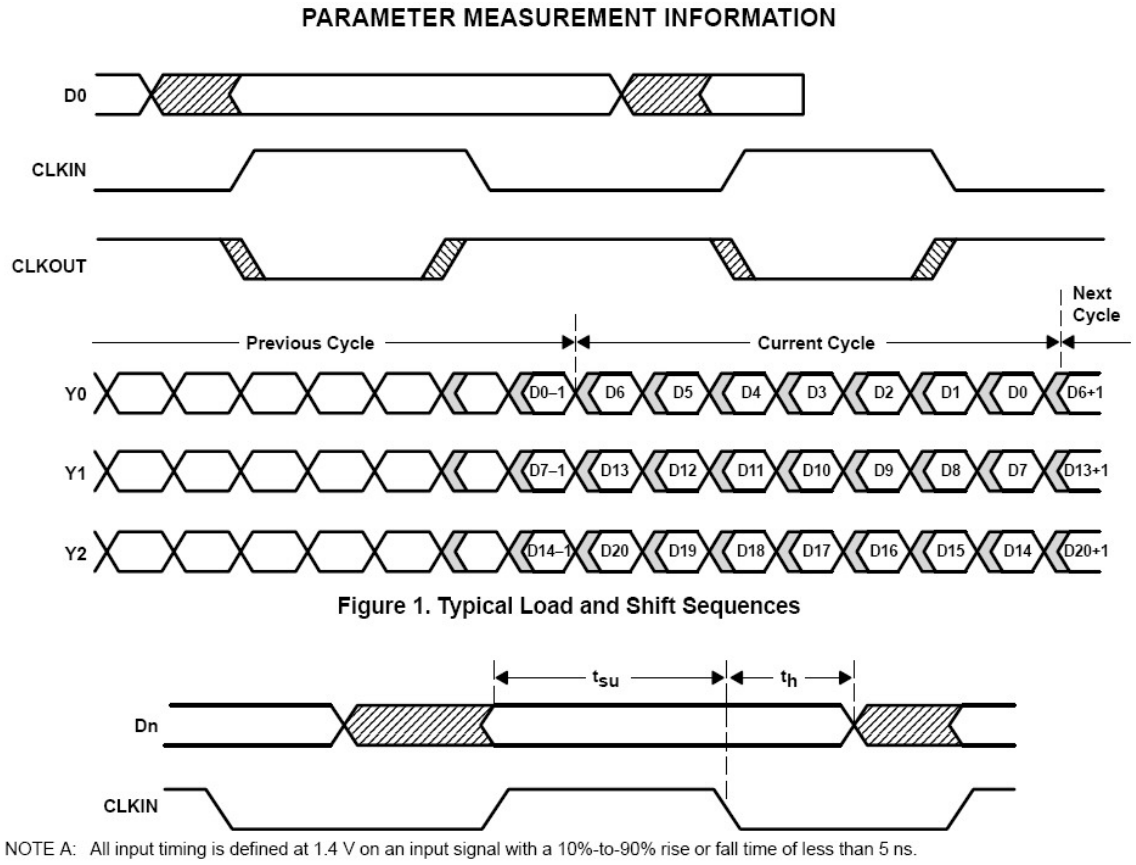


Figure 8: Parameter Measurement Information